THE SIGNIFICANCE OF POST OXIDATION ANNEALING AND POST METALLIZATION ANNEALING TO C–V CHARACTERIZATION OF Si_3N_4 MOS CAPACITOR

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ABSTRACT

The significance of post oxidation annealing (POA) and post metallization annealing (PMA) to the high frequency (1 MHz) capacitance-voltage characteristic of Si_3N_4 MOS capacitor were discussed. The MOS capacitors were fabricated with different insulator thickness by varying the deposition time (1 hour and 2 hours) of PECVD system. The capacitors underwent the POA treatment at 1000°C for 1 hour or PMA treatment at 250°C for 30 minutes. The significance of POA and PMA were determined from the shift of the experimental C-V characteristics in comparison with the ideal theoretical C-V characteristics. The shift is taken as due to the total oxide charge, Q_o in the Si_3N_4 layer of the MOS capacitors. The improvement of Si_3N_4 layer quality was observed in capacitor with PMA treatment but not in capacitor with POA treatment. The amount of oxide charges, N_o were in magnitude of 10^{12} cm^{-2}, considered large for acceptable MOS devices.

Key words: *Post Oxidation Annealing, Post Metallization Annealing, Si_3N_4 MOS Capacitor, C-V Characteristics*

INTRODUCTION

Capacitance-voltage (C – V) characterization on metal-oxide-semiconductor MOS capacitor provides further understanding of the electrical behavior of the MOS system. In the case of non-ideal structures, the C–V curve can be shifted along the voltage axis. The shift is generally attributed with the presence of oxide charge, Q_o in the oxide. In this study, Q_o is referred to total oxide charge in Si_3N_4 layer. Figure 1 illustrates the parallel shift along the voltage axis of a high-frequency C-V curve in a p-type MOS capacitor with the presence of Q_o within the oxide. The voltage shift is measured with respect to an ideal high-frequency C-V curve.

Positive Q_o causes the C-V curve shifted to more negative values of gate bias with respect to the ideal C-V curve. For negative Q_o, the C-V curve is shifted to more positive values of gate bias with respect to the ideal C-V curve.

EXPERIMENT

The process starts with wafer cleaning using passive and RCA cleaning. The Si_3N_4 layer deposition is performed using PCVD system with total flow of reactive gases is 50sccm for NH_3 and SiH_4 gas respectively, substrate heating at 280°C and 40 watt of RF power. Aluminum is deposited on top of wafer surface using electron beam evaporation technique. The gate formation is done by transferring pattern on the aluminum layer at which the unwanted portion is then removed by aluminum etching. After smoothing up the backside of the wafer by lapping, metallization is done once again to form back contact. The C – V measurement is done at high frequency (1 MHz). Except for as grown samples, the samples prepared undergo one of the heat treatments as follows:

1) Post Oxidation Annealing (POA)
   After PECVD process, samples are heated in the furnace at 1000°C for 1 hour with N_2 gas passing through the quartz tube continuously.

2) Post Metallization Annealing (PMA)
   The PMA treatment is conducted after back contact formation where the samples are heated in a furnace at 200°C for 30 minutes with N_2 gas ambient.

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The fabrication processes methodology is shown in Figure 2.

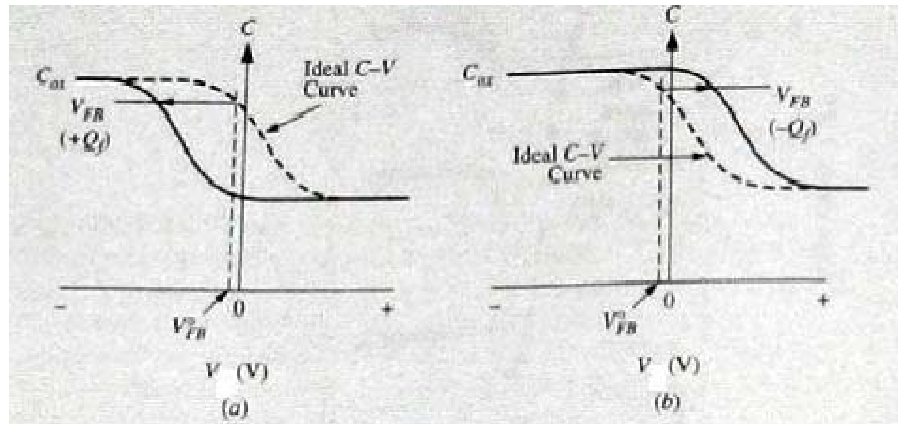


Figure 1: Shift of the high-frequency C-V curve along the voltage axis in a p-type MOS capacitor. (a) Positive oxide charge. (b) Negative oxide charge.

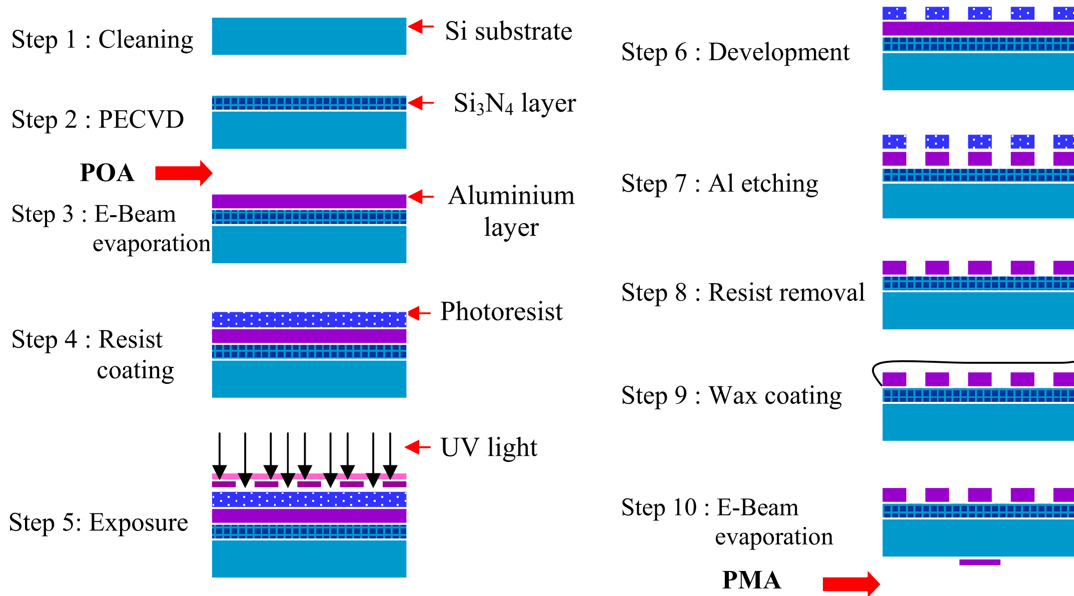


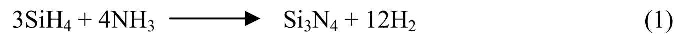
Figure 2: Fabrication processes methodology

RESULTS

The results of the C – V measurements are presented in Table 1. Δ V_{FB} indicates the additional amount of gate voltage need to be applied to achieve flat-band condition and Δ V_{Tp} indicates the additional amount of gate voltage need to be applied to achieve the onset of strong inversion.

Figure 3 (a) and (b) show the comparison between the ideal theoretical and experimental C - V characteristics for as grown sample (without POA or PMA) using 1 hour and 2 hours deposition time respectively. From the comparison of the ideal and experimental C – V characterization, negative shift for 1 hour deposition indicates positive oxide charges, Q_o while positive shift indicates negative oxide charges, Q_o. Instable PECVD deposition process which comes from contamination in PECVD chamber and insufficient supply of silane, SiH_4 gas results

in instable electronic characteristics of total oxide charges, Q_o present in Si_3N_4 layer. Thus, polarity difference of Q_o is observed for 1 hour and 2 hours deposition time. The amount of oxide charges, N_o in the range of 1.47 to 3.95×10^{12} are considered large which should be kept below 10^{10} cm^{-2} to produce acceptable MOS devices. During Si_3N_4 deposition, the chemical reaction involves is:



$$3SiH_4 + 4NH_3 \longrightarrow Si_3N_4 + 12H_2 \quad (1)$$

Since both SiH_4 and NH_3 bonds must be broken to form Si_3N_4 layer, the dangling bonds density is higher in Si_3N_4 compare to in SiO_2. Besides the higher dangling bonds density in Si_3N_4 layer, contamination of PECVD chamber contributes to the large N_o values.

Table 1: Oxide charge density, N_o for p-type Si_3N_4 MOS capacitor

PECVD	Sample	C_o (pF)	d ($\times 10^{-8}$) cm	ΔV_{FB} (V)	ΔV_{Tp} (V)	Q_o ($\times 10^{-7}$) C/cm^2	N_o ($\times 10^{12}$) cm^{-2}
	As grown	45.75	1198	-17.48	8.3	6.33	3.95
1 hour	POA	51.51	1064	-19.19	15.35	6.95	4.34
	PMA	45.75	1198	-15.87	9.45	5.75	3.59
	As grown	31.77	1722	9.33	12.96	-2.35	-1.47
2 hour	POA	39.18	1398	-14.19	9.98	3.57	2.23
	PMA	31.77	1722	-2.53	4.85	0.64	0.40

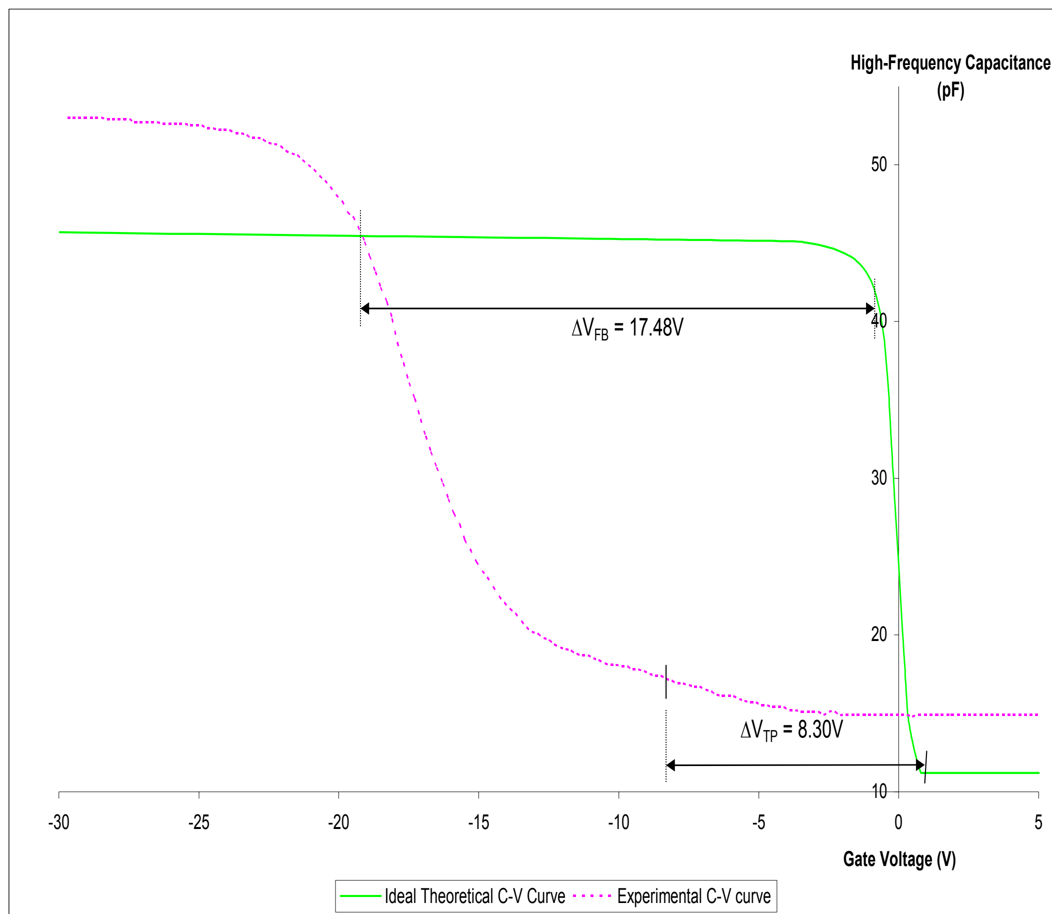


Figure 3(a): The comparison of the ideal theoretical and experimental C-V characteristic (1 hour deposition time).

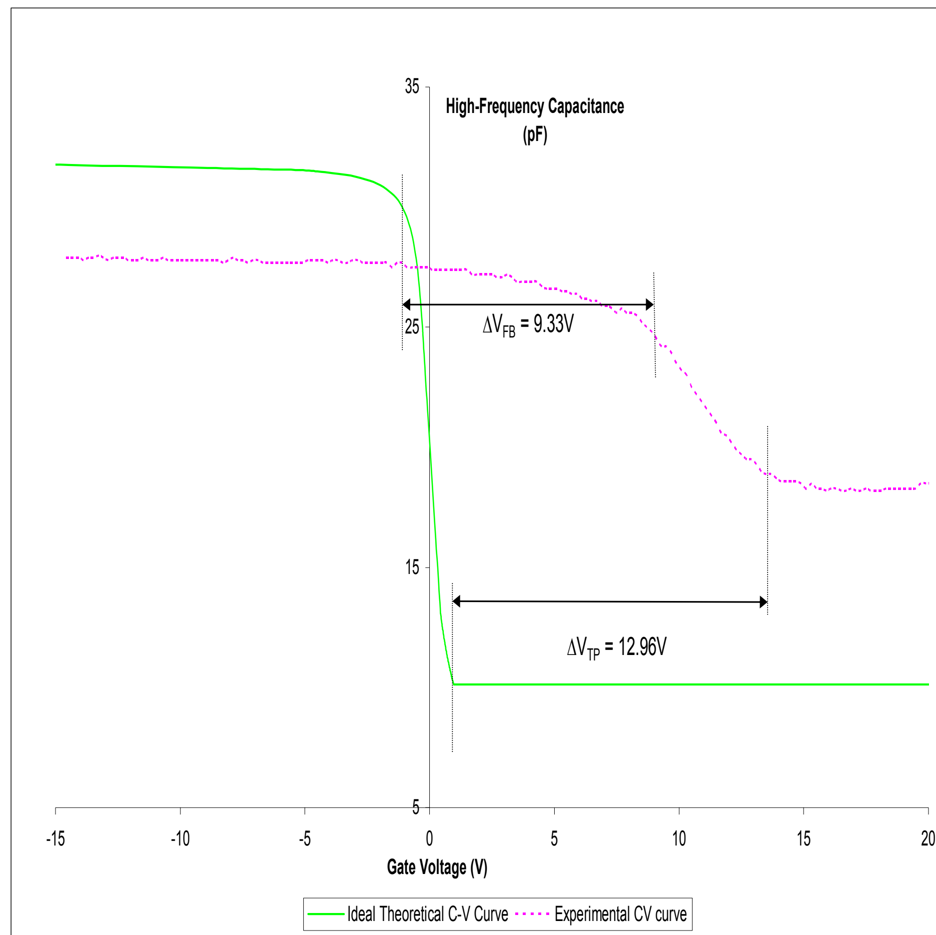


Figure 3(b): The comparison of the ideal theoretical and experimental C-V characteristic (2 hours deposition time).

Figure 4 (a) and (b) show the comparison of the experimental C-V characteristics between as grown sample and sample with POA treatment for 1 hour and 2 hours deposition time respectively. The C - V curve for sample that has gone through POA process is shifted more to the left compare to the C - V curve of sample without POA which indicates increase of N_o value for both 1 hour and 2 hours deposition time. During POA, restructuring of atomic structure takes place where the dangling bonds tend to form bonds with any nearby dangling bonds. The mechanical strength of Si_3N_4 is primarily influenced by the presence of trapped charges. As more trapped charges present in Si_3N_4 layer, the Si_3N_4 mechanical strength is weaker. At high temperature (1000°C), restructuring process destroys the atomic structure of Si_3N_4 layer and thus, results in more oxide charges, Q_o. Due to weaker structure and thicker Si_3N_4 layer obtained from 2 hours deposition time, the high temperature POA process causes the Si_3N_4 film collapses. This happens due to the presence of many dangling bonds originated from incomplete bonding. Thus, restructuring process not only destroys the atomic structure of Si_3N_4 film but also changes the electronic characteristic of the total oxide charges from negative to positive.

The comparison of the experimental C - V characteristics between as grown sample and sample with PMA treatment for 1 hour and 2 hours deposition time are shown in Figure 6 (a) and (b), respectively. C - V characteristics of PMA lies between the ideal theoretical and the experimental C - V characteristics of as grown which indicates N_o values reduce to 3.59 and 0.40×10^{12} cm^{-2} respectively for 1 hour and 2 hours deposition time.

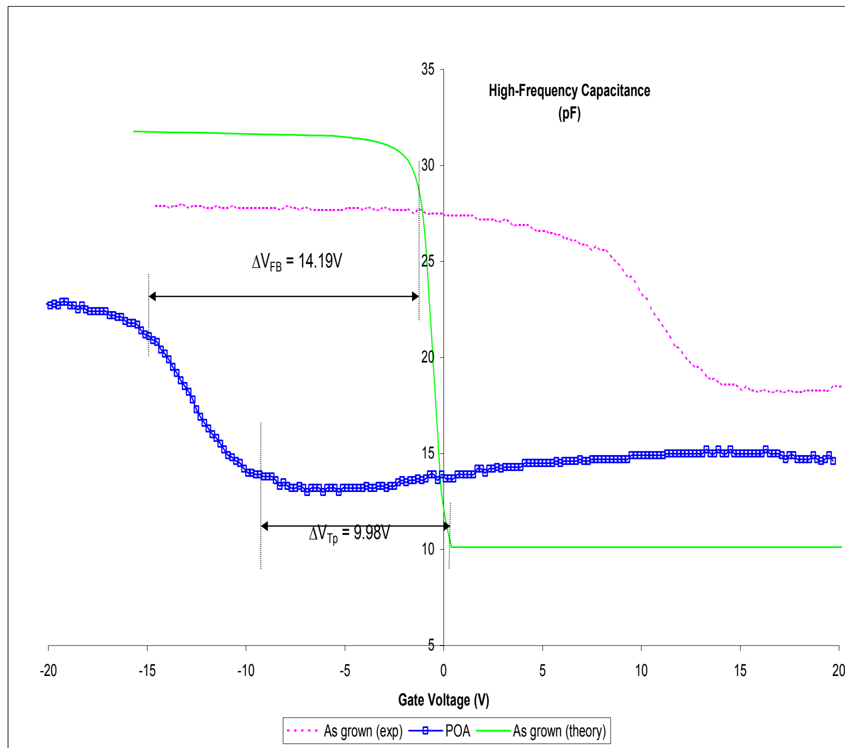


Figure 4(a): The comparison of the as grown C-V characteristics and POA C-V characteristic (1 hour deposition time).

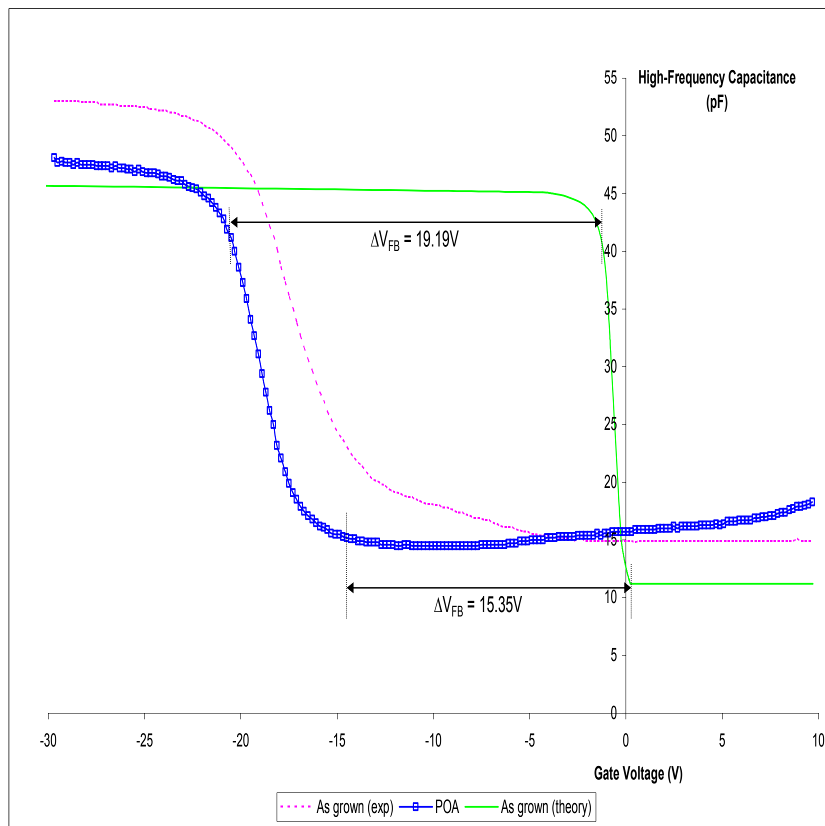


Figure 4(b): The comparison of the as grown C-V characteristics and POA C-V characteristic (2 hours deposition time).

Since the PMA temperature (200°C) is about the same temperature with PECVD deposition process (280°C), both processes mechanism are same. The broken bonds in PECVD process are used to deposit Si_3N_4 layer while in PMA treatment, the broken bonds are used to repair the structure of Si_3N_4 layer. The damaged region and disorder cluster of the Si crystal due to evaporation process is also repaired by the PMA process. Therefore, annealing process also repairs the electronic characteristics of the capacitor and restores the mobility of electron and holes. By annealing, the gap between metal and Si_3N_4 layer is reduced. So, the metal can adhere properly on the oxide surface and thus improves the electrical contact between metal and Si_3N_4 layer.

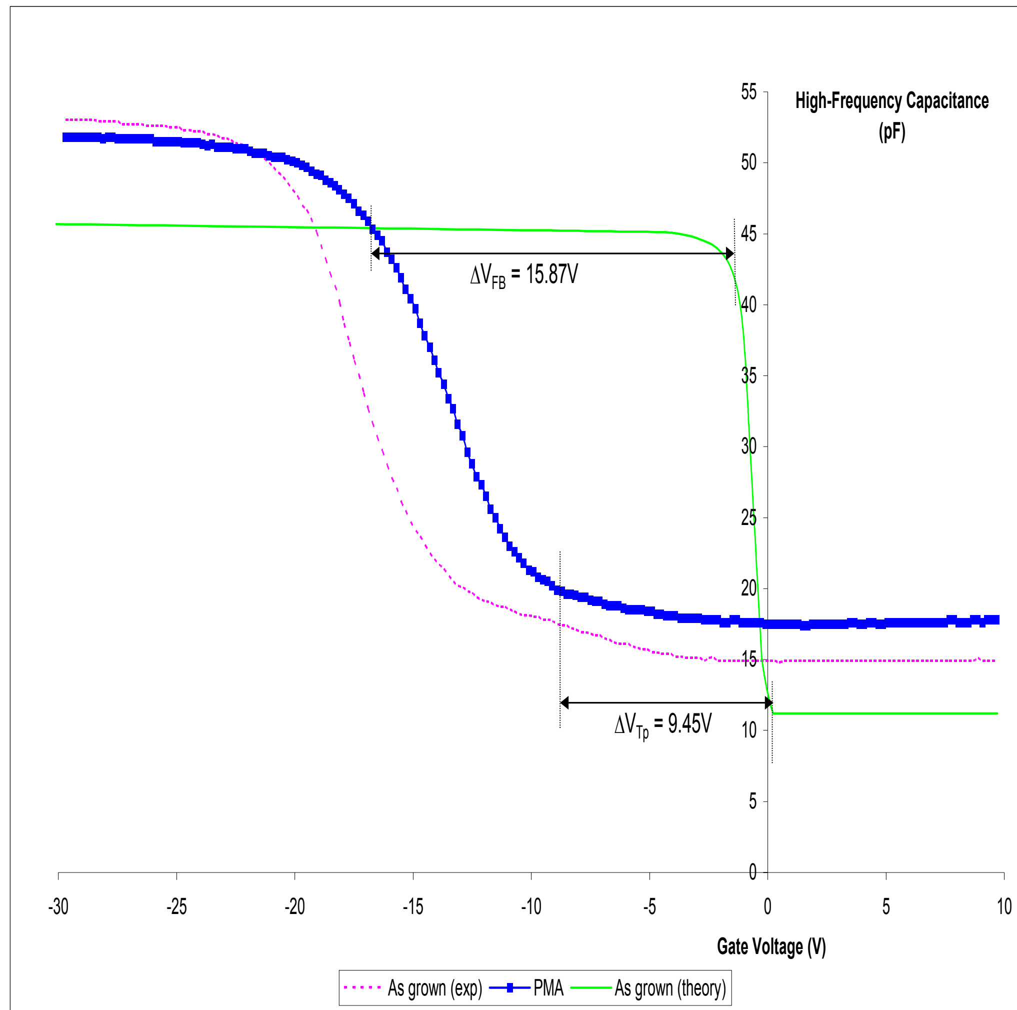


Figure 5(a): The comparison of the as grown C-V characteristics and PMA C-V characteristic (1 hour deposition time).

From Figure 4 and 5, the oxide capacitance values (the maximum capacitance values at each C – V curve) are varies from the oxide capacitance value for the ideal theoretical C – V curve. This phenomenon is more significant in sample with 2 hours deposition time compare to 1 hour deposition time. The formation of Si-N bonds is limited due to insufficient supply of SiH_4 gas. The presence of many nitrogen dangling bonds results in weak structure of Si_3N_4 film. Sample with 2 hours deposition time has weaker Si_3N_4 structure compare to sample with 1 hour deposition time since the former has more dangling bonds than the latter. During heat treatment, the Si_3N_4 weak structure cause Si_3N_4 layer collapses which reduces Si_3N_4 layer thickness. The reduced thickness results in difference in oxide capacitance values (since $C`_o = \varepsilon_{ox}/d$). The collapse phenomenon is more significant for sample with 2 hours deposition time due to weaker structure and thicker Si_3N_4 layer. From the results obtained, we can conclude that improvement of Si_3N_4 layer quality is observed for sample with PMA treatment for both 1 hour and 2 hours deposition time. High temperature (1000°C) POA treatment is not suitable for low temperature (280°C) PECVD deposited Si_3N_4 layer.

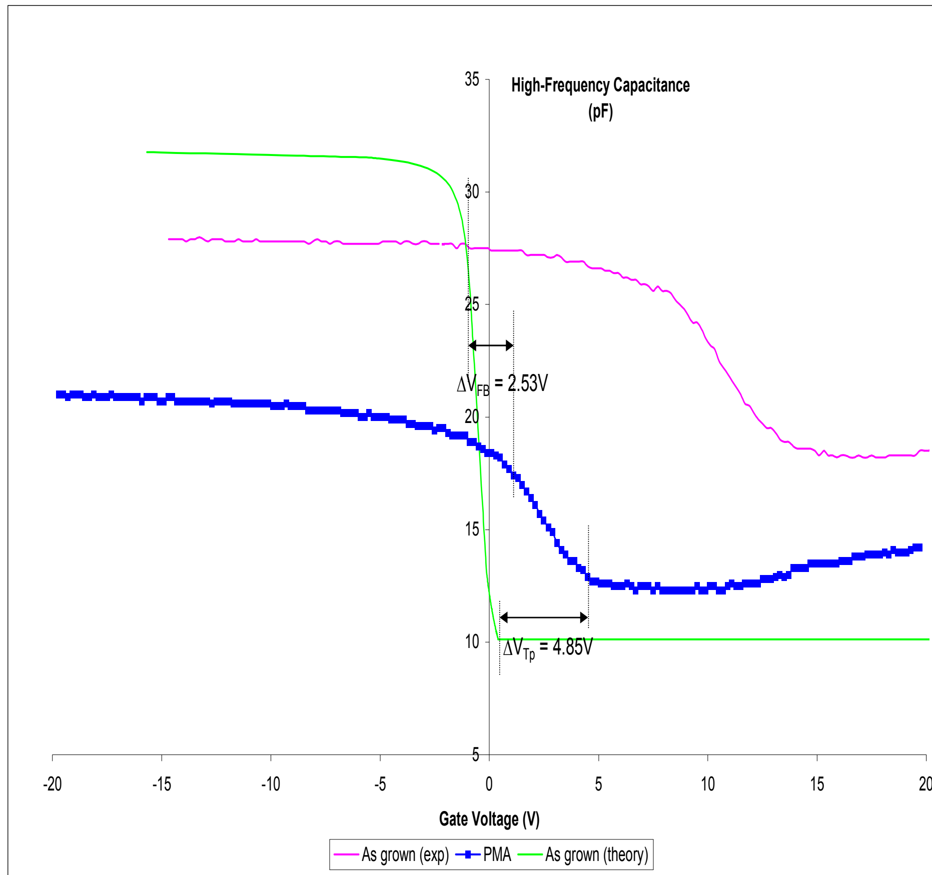


Figure 5(b): The comparison of the as grown C-V characteristics and PMA C-V characteristic (2 hours deposition time).

CONCLUSION

The PMA treatment in N_2 gas at 200°C for 30 minutes is the most significance treatment in minimizing the oxide charge, Q_o in Si_3N_4 MOS capacitor. Reduced temperature of POA treatment may gives better results on the capacitance – voltage characterization of PECVD deposited Si_3N_4 MOS capacitor.

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